INTEGRATED, STEP-DOWN SWITCHING REGULATOR

Device Type	Current Rating	Input Voltage	Output Voltage
VT225	12A	3.3V	1.0V to 2.6V
	14A	5.0V	

GENERAL DESCRIPTION

The VT225 is a fully integrated, highly efficient switching regulator for applications operating from 2.97V to 5.5V requiring up to 14A maximum load. These single-chip regulators provide an extremely compact, fast, and accurate power delivery solution for low output voltage applications.

Requiring few external components, they are ideal for space-constrained applications. A 14A solution, for example, occupies a board space less than 170mm^2 with a height less than 3mm to 5mm depending on the inductor choice. Over- and undervoltage lockout, chip enable input, and a status signal are provided.

These regulators allow designers to program power good levels, switching frequency/inductor ripple current, output impedance and maximum output power. The programmable features can be used to make trade-offs between the voltage regulator's performance and cost. Also provided are default settings for these parameters that optimize for smallest footprint and best transient performance.

The proprietary control scheme features cycle-by-cycle current limiting with short-circuit protection and supports dynamic load transients of over 300A/µs at greater than 90% efficiency. Output voltage is adjustable down to 1.0V, and the regulator has remote sense capability for optimal point-of-load regulation. Two chips may be connected in parallel for larger loads with adjustable current sharing among chips.

BASIC APPLICATION CIRCUIT

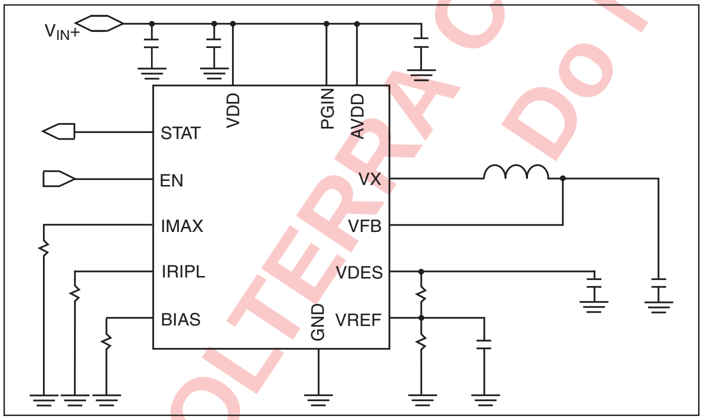


Figure 1. High Efficiency Buck Regulator

KEY FEATURES

- Smallest Footprint Solution
- Lowest Profile Solution: 3mm to 5mm Maximum Height
- Highest Efficiency Solution: Up to 97% Peak Efficiency
- Ultra-Fast Transient Response: Supports >300A/µs Step Load Transients
- Minimum Output Capacitance
- Sources Current
- Scalable for Higher Current Applications
- High Frequency Operation: Up to 2MHz

ADDITIONAL FEATURES

- Supports Differential Remote Sense
- Integrated Soft Start
- Cycle-by-Cycle Current Limiting
- Short Circuit Protection
- Undervoltage and Overvoltage Lockout
- Programmable Power Good Indicator
- Supports Voltage Margining
- Chip Enable
- Thermal Shutdown with Hysteresis
- Programmable Frequency and Output Impedance

SYSTEMS

- Broadband Communication
- Networking
- Enterprise Storage
- Servers and Workstations
- Notebook Computers

APPLICATIONS

DC-DC Converter Modules and On-Board, Point-of-Load Voltage Regulators

- Network Processors
- FPGAs and DSPs
- Switch Fabric ASICs
- I/O: Infiniband, Ethernet and Fibre Channel
- Memory and Bus Termination
- Micro-Controllers
- Graphic Processors
- µP Chipsets
- RAID Controllers

INTEGRATED, STEP-DOWN SWITCHING REGULATOR

ORDERING INFORMATION

Part Number	Current Level	Package	Drawing Number	Shipment Method	Package Marking
VT225CR-ADJ	14A	CSP-62	ES AP-0652	250u Tape & Reel	VT225
VT225CX-ADJ				2.5ku Tape & Reel	

ABSOLUTE MAXIMUM RATINGS (SEE NOTE 2)

Input Pin Voltages .... -0.3V to 7V
Junction Temperature (T_J).. 150°C
Storage Temperature Range .... -65°C to 150°C
Peak Reflow Temperature (30 - 90 Sec).................. 240°C

NOTE 1: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

OPERATING RATINGS

Input Voltage (V_{DD} & A_{VDD}) ....2.97V to 5.5V
Junction Temperature (T_J)..............................0°C to 125°C
VT225 Output Current (I_{OUT})....................................... 14A

THERMAL RATINGS

Θ_{JC} (Max) ....1°C/W

ELECTRICAL CHARACTERISTICS

$A_{VDD} = V_{DD}$ = 3.3V ± 10% and 5.0V ±10% unless otherwise specified. The ✻ denotes specifications which apply over the full operating junction temperature range (T_J = 0 to 125°C), otherwise specifications are for T_J = 25°C.

Symbol	Parameter	Conditions			Min	Typ	Max	Units
Supply Voltages, V_{DD} & A_{VDD}								
V_{DD}	FET Input Voltage Range				2.25		A_{VDD} + 0.3	V
A_{VDD} & V_{DD}	Input Voltage Range			✻	2.97		5.5	V
I_{DD}	Input DC Supply Current	I_{OUT} = 0A, Fsw = 1.5MHz				80		mA
Output Voltage								
V_{OUT}	Output Voltage Range			✻	1.0		2.6	V
Reference Voltage								
-	Output Voltage Range			✻	1		2.6	V
-	DC Accuracy	$R_{BIAS} = R_{REF}$ = 43.2kΩ, ±0.1%		✻	-1%	1.23	+1%	V
Current Limit								
I_{LIM}	Peak Current Limit	Default Setting				15		A
$I_{AVG-MAX}$	Average Current Limit	$I_{MAX} = A_{VDD}$			14			A
Regulation and System Specifications (Specified by design, tested using circuit in Figure 8)								
-	Line Regulation	V_{DD} = 3.3V ±10%				1		mV
-	Line Regulation	V_{DD} = 5V ±10%				7		mV
-	Load Regulation	R_{FB} = 0Ω, I_{OUT} = 0 to 12A				3		mV
-	Output Ripple	R_{RIPL} = 24.8kΩ, V_{DD} = 3.3V				15		mVp-p
SR_{OUT}	Output Slew Rate					300		A/µs
Eff	Efficiency	Fsw = 1MHz, I_{OUT} = 14A, V_{DD} = 5V	V_{OUT} = 1.2V			86		%
			V_{OUT} = 2.5V			92		%
Pd	Total System Power Dissipation	V_{OUT} = 1.2V, I_{OUT} = 14A	V_{DD} = 3.3V			2.5		W
			V_{DD} = 5V			2.7		W

INTEGRATED, STEP-DOWN SWITCHING REGULATOR

ELECTRICAL CHARACTERISTICS (CONTINUED)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Undervoltage Lockout						
$UVLO1_{UPPER}$	VDD Undervoltage Lockout Upper Threshold			2.2		V
$UVLO1_{LOWER}$	VDD Undervoltage Lockout Lower Threshold			2.0		V
$UVLO2_{UPPER}$	AVDD Undervoltage Lockout Upper Threshold			2.8		V
$UVLO2_{LOWER}$	AVDD Undervoltage Lockout Lower Threshold			2.7		V
Overvoltage Lockout						
$OVLO_{UPPER}$	VDD Overvoltage Lockout Upper Threshold			6.3		V
$OVLO_{LOWER}$	VDD Overvoltage Lockout Lower Threshold			6.0		V
Status Pin						
$V_{OL\text{-}STAT}$	Status Output Low Voltage	I_{OUT} = 4mA			0.4	V
$I_{OL\text{-}STAT}$	Status Current Sink Capability	V_{OUT} = 0.2V	4	10		mA
Output Enable Pin						
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
$I_{IN\text{-}LLH}$	Input Current - Logic Level High	V_{IN} = 5V		4.5	10	µA
IMAX Pin (Programmable)						
$I_{MAX\text{-}DEFAULT}$	Default Current	No Programming Resistor (Default Condition)		120		µA
$I_{IN\text{-}IMAX\text{-}MIN}$	Minimum Input Current	With Programming Resistor		5		µA
$I_{IN\text{-}IMAX\text{-}MAX}$	Maximum Input Current	With Programming Resistor		150		µA
$V_{OUT\text{-}IMAX}$	Output Voltage			1.23		V
$V_{TH\text{-}IMAX}$	Disable Threshold Voltage	No Programming Resistor (Default Condition)		A_{VDD} - 1		V
IRIPL Pin (Programmable)						
$I_{IRIPL\text{-}DEFAULT}$	Default Current	No Programming Resistor (Default Condition)		50		µA
$I_{IN\text{-}IRIPL\text{-}MIN}$	Minimum Input Current	With Programming Resistor		5		µA
$I_{IN\text{-}IRIPL\text{-}MAX}$	Maximum Input Current	With Programming Resistor		150		µA
$V_{OUT\text{-}IRIPL}$	Output Voltage			1.23		V
$V_{TH\text{-}IRIPL}$	Disable Threshold Voltage	No Programming Resistor (Default Condition)		A_{VDD} - 1		V
BIAS Pin						
I_{BIAS}	BIAS Current	With R_{BIAS}	20		40	µA
$V_{OUT\text{-}BIAS}$	Output Voltage			1.23		V
$V_{TH\text{-}BIAS}$	Disable Threshold Voltage	Without R_{BIAS}		A_{VDD} - 1		V

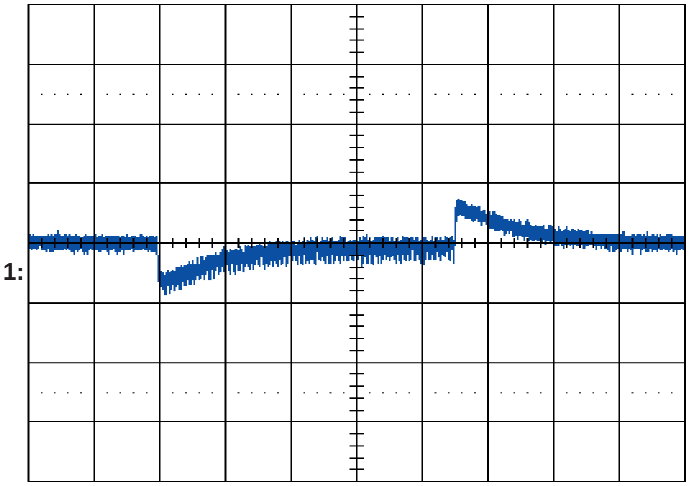
ELECTRICAL CHARACTERISTICS (CONTINUED)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
Error Amplfier (VFB & VDES)							
$V_{IN\text{-}OS}$	Input Offset Voltage		*			±3.5	mV
Z_{OUT}	High-Frequency Output Impedance				330		Ω
τ	Integrator Time Constant				30		µs
$I_{OUT\text{-}MAX}$	Maximum Output Current				1		mA
V_{CM}	Common Mode Input Voltage Range			0.5		A_{VDD} - 0.85	V
Switching Current Amplfier							
Ki	Current Gain				120,000		
Power Good Amplfier (PGIN & VREF)							
$V_{IN\text{-}OS}$	Input Offset Voltage					±10	mV
Z_{OUT}	Output Impedance				1000		Ω
$I_{TH\text{-}N}$	Negative Threshold Current				10		µA
$I_{TH\text{-}P}$	Positive Threshold Current				10		µA
$I_{TH\text{-}HYST}$	Threshold Current Hysterisis				1		µA
$I_{OUT\text{-}MAX}$	Maximum Output Current				250		µA
V_{CM}	Common Mode Input Voltage Range			0.5		A_{VDD} - 0.85	V
Thermal Shutdown (Specified by Design)							
$T_{SHDN\text{-}R}$	Rising Threshold				145		°C
$T_{SHDN\text{-}F}$	Falling Threshold				120		°C

INTEGRATED, STEP-DOWN SWITCHING REGULATOR

TYPICAL OPERATING CHARACTERISTICS (REFERENCE FIGURE 8 SCHEMATIC)

Transient Response

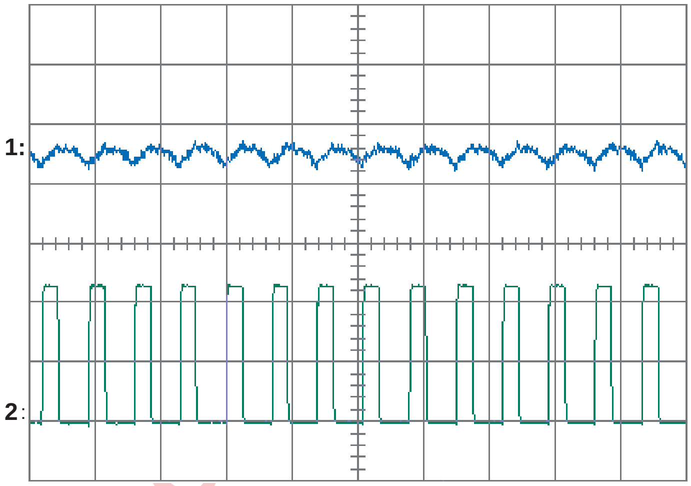


Time/Div: 20µs

Conditions: V_{IN} = 5V
V_{OUT} = 1.8V
I_{OUT} = 9 - 14A Load Step
Slew Rate = 300A/µs

1: Output (20mV/div)

Output Voltage Ripple

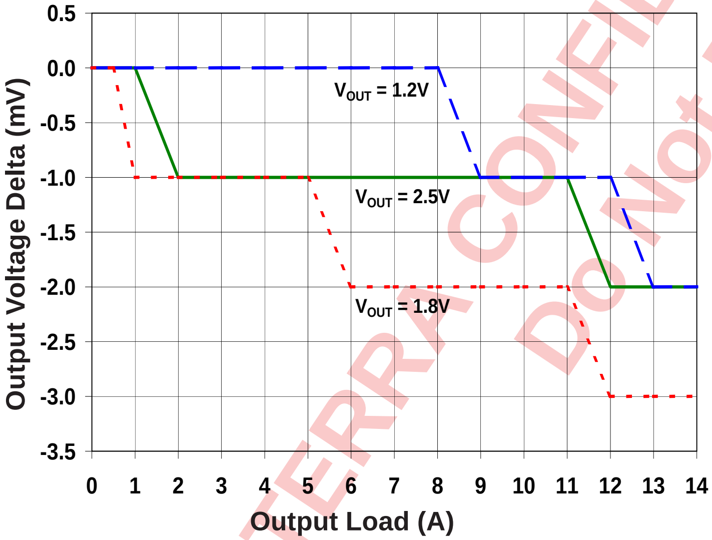


Time/Div: 1µs

Conditions: V_{IN} = 5V
V_{OUT} = 1.5V
I_{OUT} = 14A

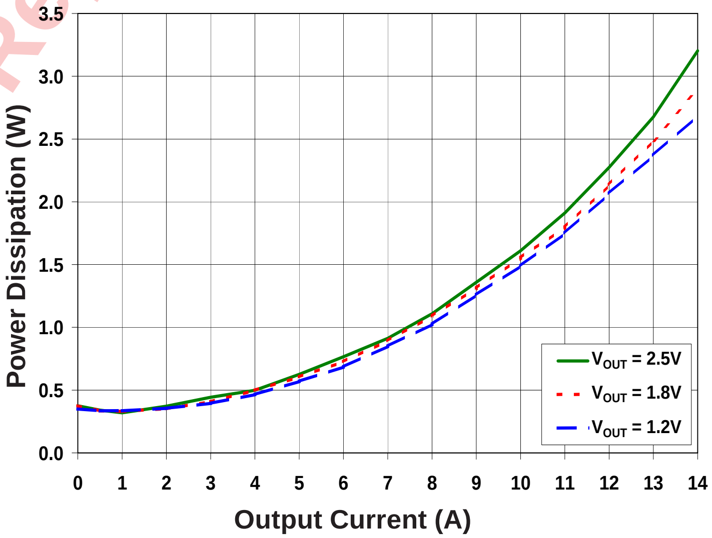
1: Output (20mV/div)
2: V_X (2V/div)

Load Regulation



Conditions: V_{IN} = 5V
V_{OUT} = 1.5V
Fsw = 1MHz
T_A = 25°C

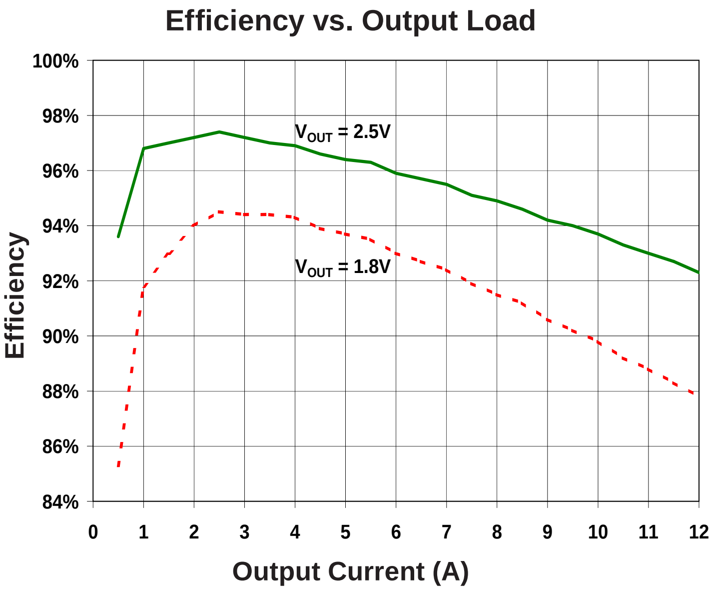
Power Dissipation vs. Output Current



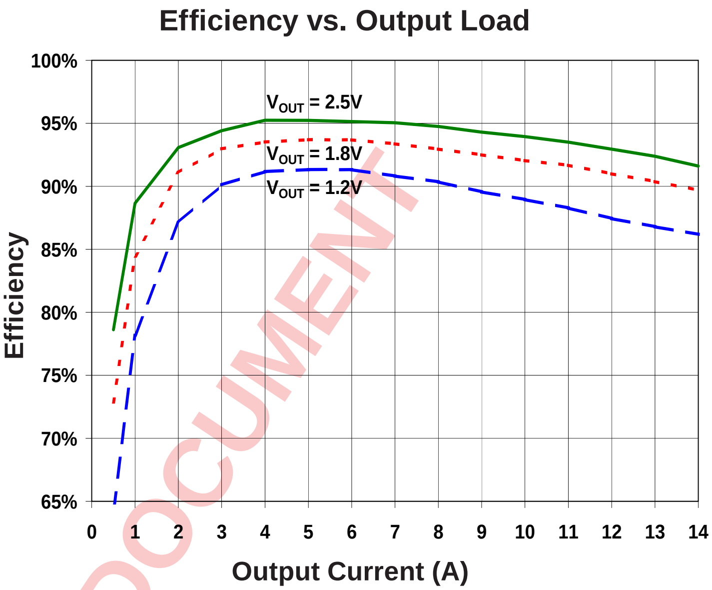
Conditions: V_{IN} = 5V
Fsw = 1MHz
L = 200nH
T_A = 25°C

INTEGRATED, STEP-DOWN SWITCHING REGULATOR

TYPICAL OPERATING CHARACTERISTICS (CONTINUED)

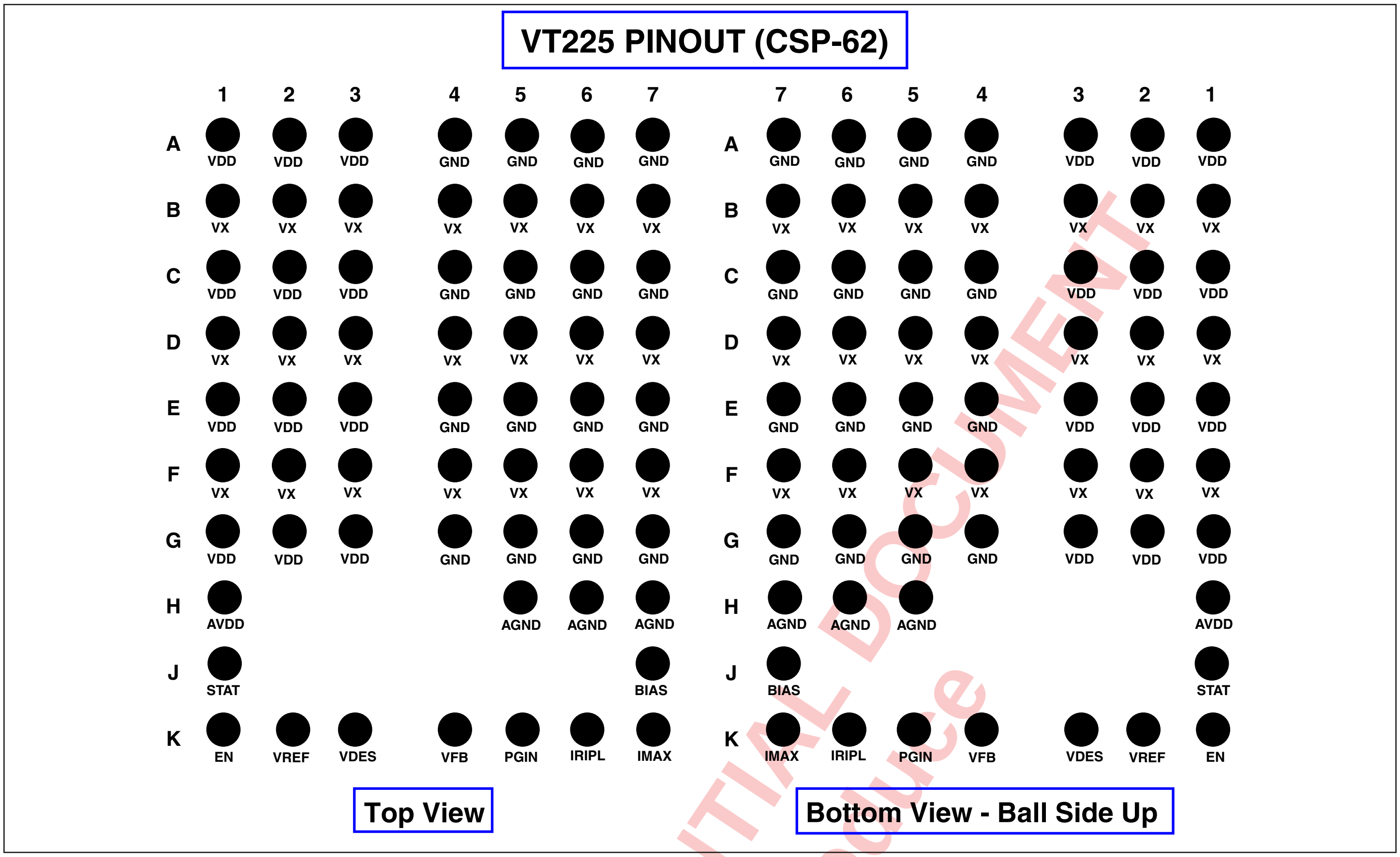


Conditions: V_{IN} = 3.3V
Fsw = 1MHz
L = 200nH
T_A = 25°C



Conditions: V_{IN} = 5V
Fsw = 1MHz
L = 200nH
T_A = 25°C

INTEGRATED, STEP-DOWN SWITCHING REGULATOR



VT225 PINOUT (CSP-62)

Top View

	1	2	3	4	5	6	7
A	VDD	VDD	VDD	GND	GND	GND	GND
B	VX	VX	VX	VX	VX	VX	VX
C	VDD	VDD	VDD	GND	GND	GND	GND
D	VX	VX	VX	VX	VX	VX	VX
E	VDD	VDD	VDD	GND	GND	GND	GND
F	VX	VX	VX	VX	VX	VX	VX
G	VDD	VDD	VDD	GND	GND	GND	GND
H	AVDD				AGND	AGND	AGND
J	STAT						BIAS
K	EN	VREF	VDES	VFB	PGIN	IRIPL	IMAX

Bottom View - Ball Side Up

	7	6	5	4	3	2	1
A	GND	GND	GND	GND	VDD	VDD	VDD
B	VX	VX	VX	VX	VX	VX	VX
C	GND	GND	GND	GND	VDD	VDD	VDD
D	VX	VX	VX	VX	VX	VX	VX
E	GND	GND	GND	GND	VDD	VDD	VDD
F	VX	VX	VX	VX	VX	VX	VX
G	GND	GND	GND	GND	VDD	VDD	VDD
H	AGND	AGND	AGND				AVDD
J	BIAS						STAT
K	IMAX	IRIPL	PGIN	VFB	VDES	VREF	EN

CONNECTION INFORMATION

VDD: Input supply voltage node. These balls connect to the input power supply source.

GND: Ground node. These balls connect directly to the ground plane.

VX: Switching node. These balls connect the switching node of the power devices to the output inductor.

AVDD: Analog power supply voltage. This ball connects to the input power supply source through an external RC filter.

AGND: Power analog ground node. These balls connect to analog ground.

STAT: Status pin. When this pin is HIGH, the chip is functioning within normal operating parameters. This open-drain output must be externally pulled HIGH. (See the Regulator Status section for more information).

BIAS: Used to generate internal bias currents. Connect a 43.2kΩ resistor between this pin and AGND. If the user wishes to overdrive VREF with an external reference, connect BIAS to AVDD. (See the Control Architecture section for more information.)

EN: Output enable pin. When this pin is HIGH, the output voltage is enabled. When this pin is LOW, the output voltage is disabled. This pin is internally pulled LOW.

VREF: Voltage reference pin. To generate an accurate reference voltage, connect a resistor with 1% or better tolerence between this pin and the load ground. If using an external reference, connect BIAS to AVDD or ensure the external reference is capable of sinking >30µA of current. (See the Control Architecture section for more information.)

VDES: Desired output voltage pin. The regulator will adjust the output voltage to track the voltage on this pin.

VFB: Output voltage feedback pin. This pin provides an output voltage feedback connection to the regulator.

PGIN: Resistor sense to set power good voltage tolerance. If this feature is not desired, this ball should be connected to AVDD.

PROGRAMMING PINS

IRIPL: Ripple current pin. This pin is used to set peak-to-peak ripple current with a resistor to ground. A default ripple current will be selected if this ball is pulled directly to AVDD.

IMAX: Maximum average current pin. This pin enables a user to set a maximum average current to the part. A default maximum average current will be set if this ball is pulled directly to AVDD.

INTEGRATED, STEP-DOWN SWITCHING REGULATOR

OPERATION

The VT225 chip provides a highly integrated, compact solution for high-efficiency, low-voltage power conversion. The following sections describe in detail the use and operation of these regulators.

Control Architecture

A simplified block diagram is shown in Figure 2. This regulator implements a true average current mode control algorithm that achieves stable switching operation without the need for external compensation. This proprietary algorithm also enables current sharing between two or more regulators without additional components. A description of the basic control loop follows.

Voltage regulation is achieved by monitoring the difference between the desired output voltage on the VDES pin and the actual output voltage across the load, V_{OUT}. The error amplifier is connected as a voltage follower that tries to maintain the VFB pin at the same voltage as the VDES pin.

Any difference in voltage between the VFB pin and VDES causes an error current to flow through resistor R_{FB}. This error current (I_{ERROR}) is sensed in the error amplifier and fed to the Switching Current Amplifier block.

The Switching Current Amplifier block accepts four inputs: the error current signal, control logic information, the desired ripple current (I_{RIPL}), and the desired maximum average output current (I_{MAX}). The user programs the latter two signals by selecting appropriate resistor values for R_{RIPL} and R_{MAX}. The output of this block is a triangular waveform, shown in Figure 3, which appears at pin VX as the inductor output current I_{OUT}. The average value of this waveform (I_{AVG}) equals the I_{ERROR} amplified by a large gain factor, Ki (approximately 120,000). An error current of approximately 100µA, for instance, results in an average output current of 12A. The average output current adjusts the output voltage in the appropriate direction to maintain regulation. Using proprietary on-chip current sensing, the Switching Current Amplifier block also maintains a constant peak-to-peak current amplitude (equal to I_{RIPL}) that is independent of duty cycle, inductor value, input voltage,

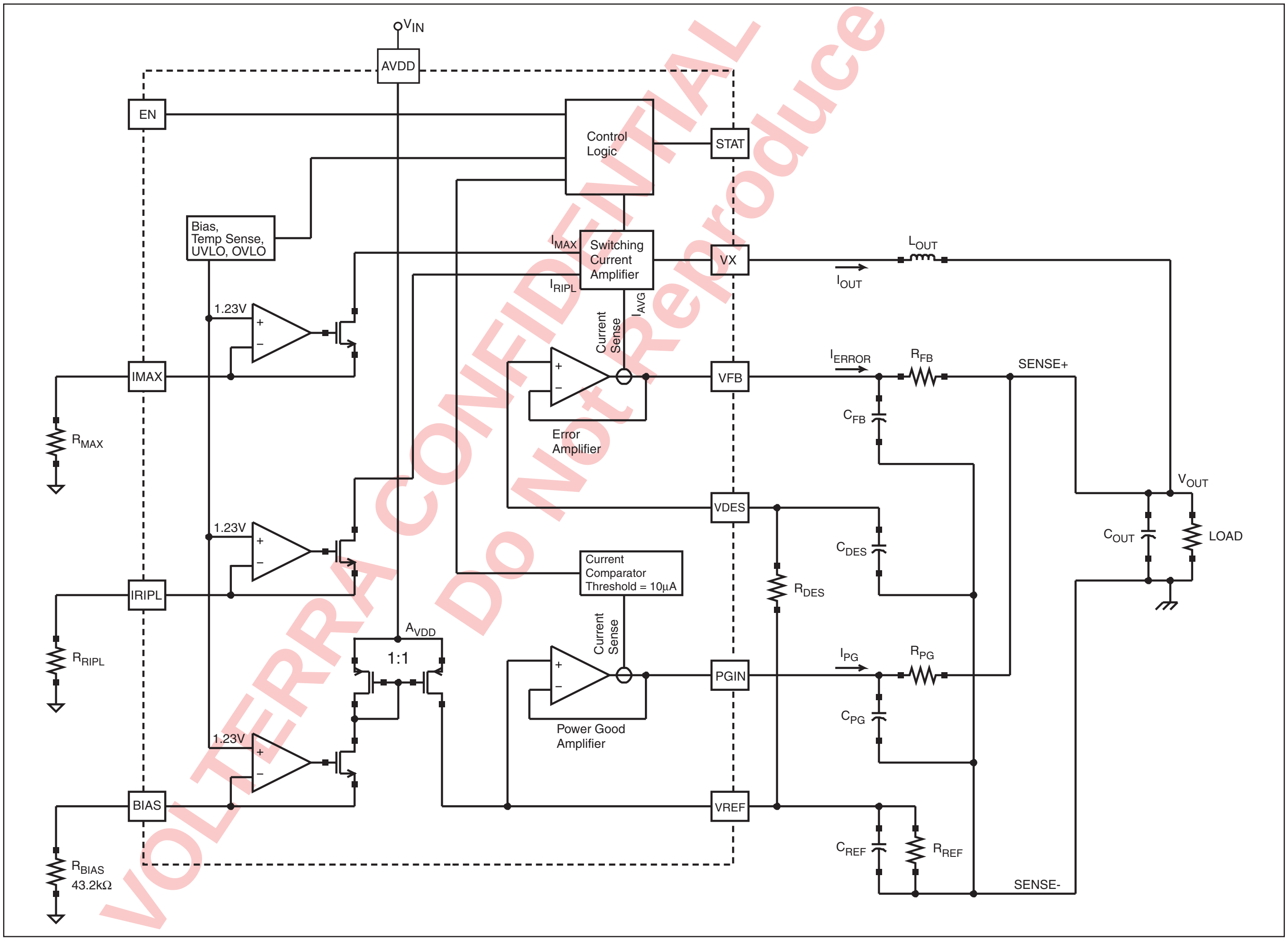


Figure 2. Functional Block Diagram

INTEGRATED, STEP-DOWN SWITCHING REGULATOR

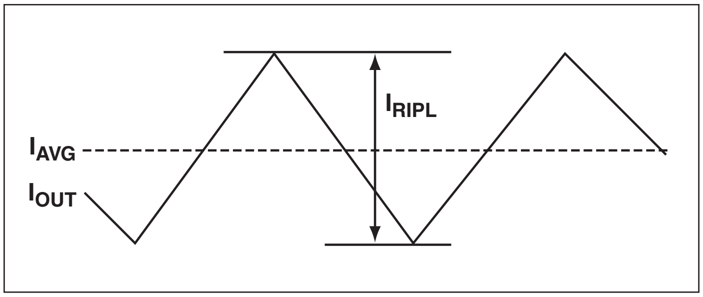


Figure 3. Output of the Switching Current Amplifier Block

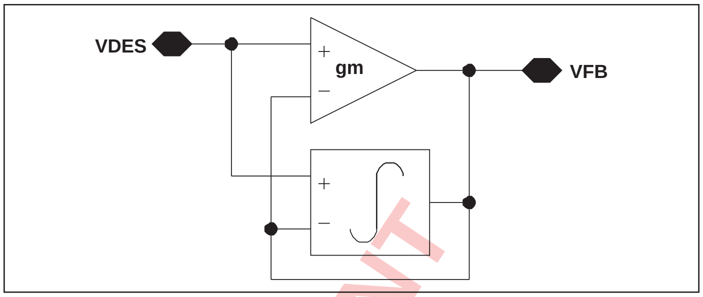


Figure 4. Block Diagram of the Error Amplifier

or output voltage. The resulting switching frequency of the converter may be approximated by the equation:

$$F_{SW} = \frac{V_{OUT} \bullet (V_{IN} - V_{OUT})}{V_{IN} \bullet L_{OUT} \bullet I_{RIPL}}$$

where V_{OUT} is the output voltage, V_{IN} is the input voltage, L_{OUT} is the output inductor, and I_{RIPL} is the peak-to-peak current amplitude. The exact frequency will tend to be higher as a result of second order effects such as the value of output capacitance, ESR and ESL. Additionally, the high side and low side switches have a minimum-on-time of about 100ns, which limits the maximum frequency that can be programmed.

The regulator's output voltage droop is programmed using an external resistor R_{FB}. The current I_{ERROR} flows through R_{FB} and generates a voltage droop at full load that is directly proportional to R_{FB}. For example, if R_{FB} is 200Ω, when $I_{OUT} = 12A$, then ~100µA of error current will cause 20mV of droop at the output. Since the Switching Current Amplifier produces a DC output current that is proportional to the error current flowing through R_{FB} and is in parallel with R_{FB}, the effective DC output resistance of the regulator is simply R_{FB} divided by the gain of the Switching Current Amplifier. The resulting voltage droop can be determined from the following equation:

$$V_{DROOP} = \left(\frac{R_{FB}}{Ki}\right) \bullet I_{OUT}$$

where Ki = 120,000.

The voltage reference circuits support output regulation above or below the bandgap reference level (1.23V). Output voltages as low as 0.5V can be generated using this regulator. Initially, a reference bias current is established by forcing the bandgap voltage at the BIAS pin across the external resistor R_{BIAS}. The R_{BIAS} resistor MUST be 43.2kΩ to create the proper bias current reference for on-chip circuitry. This bias current is mirrored and applied to the external resistor R_{REF} connected to the VREF pin, resulting in a voltage at the VREF pin given by:

$$V_{REF} = 1.23V \bullet \left(\frac{R_{REF}}{R_{BIAS}}\right)$$

V_{REF} is generated relative to the load ground, eliminating any error caused by differences in ground potential between the regulator and its load. Resistor tolerances for R_{REF} and R_{BIAS} directly affect the DC accuracy of the output voltage, so 0.1% resistors are recommended for high-accuracy applications.

The Power Good Amplifier senses V_{REF} to determine whether the output voltage is within regulator tolerance limits. More information on setting Power Good threshold limits using the external resistor R_{PG} connected to the PGIN pin is provided in the Power Good Detection section of this datasheet. In most applications, the VREF voltage is also connected directly to the VDES pin to set the desired output voltage.

Error Amplifier Operation

The error amplifier senses the error signal as a current rather than a voltage. Because of this, it is implemented as a transconductance (gm) stage in parallel with an integrator with a current output, as shown in Figure 4. The integrator provides a large DC gain and ensures that there is very little steady-state voltage error between VDES and VFB.

Even with zero static voltage error, however, there will be a momentary voltage error on VFB during a load transient due to the finite high-frequency gain of the gm stage, which is approximately 3mS (~1/330Ω). This transient voltage error will be sensed by the integrator and will decay back to zero with a time constant of approximately 30µs. The magnitude of the transient voltage error on VFB can be estimated by the following equation:

$$V_{FB}(\text{error}) = I_{LOAD}(\text{transient}) \bullet \left(\frac{330\Omega}{Ki}\right)$$

For example, a 12A load step on a VT225 with Ki = 120,000 will generate a transient voltage error of approximately 33mV that will decay away with a 30µs time constant.

The capacitor C_{FB} is used to compensate the error amplifier and its recommended value is 220pF. This capacitor is not required if VFB is connected directly to V_{OUT} (no droop application).

Maximum Output Current and Ripple Current Selection

Two programmable inputs are used to control operation of the Switching Current Amplifier: IMAX controls the maximum average output current; IRIPL controls the peak-to-peak output ripple current. Current levels are programmed using resistors connected to the IMAX and IRIPL pins. In both cases, 1.23V is forced across the programming resistors by internal amplifiers and the resulting currents are fed to the Switching Current Amplifier block. Current values are then scaled by a factor of Ki. For example, setting R_{MAX} equal to 12.3kΩ and R_{RIPL} to 24.6kΩ with a VT225 (Ki = 120,000) sets the desired maximum average output current I_{OUTMAX} to approximately 12A (= [1.23V/12.3kΩ] • 120,000) and the peak-to-peak output ripple amplitude $I_{OUTRIPL}$ to approximately 6A (=[1.23V/24.6kΩ] • 120,000).

R_{RIPL} can be used to set the switching frequency of the regulator via the following approximate equation:

$$Fsw = \frac{V_{OUT} \bullet (V_{IN} - V_{OUT})}{V_{IN} \bullet L_{OUT} \bullet I_{RIPL}}$$

where

$$I_{OUTRIPL} = Ki \bullet \left(\frac{1.23V}{R_{RIPL}}\right)$$

The high-side and low-side switches have minimum on-times of about 100ns, which limit the maximum frequency that can be programmed. The switching behavior, however, should be defined by the ripple current band and not set by minimum on-times. Thus, it is recommended that the switching behavior be programmed for on-times greater than 130ns.

If either the IMAX or IRIPL input is connected to AVDD, an internally generated default current is sent to the Switching Current Amplifier. The values of the default currents are approximately 120µA for the IMAX pin (corresponding to a maximum average output current of approximately 14.4A) and 50µA for the IRIPL pin (corresponding to a peak-to-peak ripple current of approximately 6A). These values have a tolerance of ± 25%. These default currents are also sent to the Switching Current Amplifier if there is an open or short to ground detected on either input. In these cases, the regulator still operates using the default current thresholds, but the status (STAT) signal goes LOW to indicate a problem.

If, at any time, I_{MAX} drops below a preset level of 4A, the regulator stops switching and the STAT pin goes LOW to indicate a fault condition. There are two likely causes for this error; either I_{MAX} has been programmed too low (i.e., less than 4A) or I_{RIPL} has been programmed too high, forcing the regulator's protective override to impose a correspondingly lower I_{MAX}.

Chip Enable

The chip enable (EN) signal enables or disables the regulator. EN signal HIGH enables the regulator to switch. A logic level LOW disables switching and turns off static current on the regulator. This signal is internally pulled LOW and has TTL compatible threshold levels.

Soft Start

Regulator start-up is governed by a soft start circuit that can easily be adjusted by slowing the rise time of the desired output voltage signal V_{DES} through the appropriate selection of capacitor C_{DES} in series with R_{DES}. C_{DES} also improves high-frequency sensing of the load ground. The minimum recommended value of C_{DES} is 100pF.

UVLO and OVLO Protection

This design monitors VDD with both undervoltage lockout (UVLO) and overvoltage lockout (OVLO) circuits. Similarly, AVDD is monitored by a UVLO threshold circuit. When the input supply voltage is below the UVLO thresholds or above the OVLO thresholds, the regulator stops switching, and the STAT pin is driven low. For UVLO and OVLO levels, refer to the Electrical Characteristics table.

Over Temperature Protection

If the die temperature reaches approximately 145°C during operation, a temperature sensing circuit disables the regulator and the STAT pin is driven LOW. Once the die temperature drops to approximately 125°C, the regulator resumes switching.

Current Limiting and Short Circuit Protection

The regulator's current mode control architecture provides inherent cycle-by-cycle current limiting and short circuit protection for both positive and negative output currents. Instantaneous peak currents are monitored and controlled on a cycle-by-cycle basis within the Switching Current Amplifier block. Average currents are limited by the IMAX pin.

Power Good Detection

An internal power good detection circuit can be used to detect when the output voltage is within a programmable tolerance limit. Referring to Figure 2, the Power Good Amplifier is connected as a unity-gain voltage follower that tries to maintain the PGIN pin at the same voltage as the VREF pin. Any difference in voltage between V_{REF} and V_{OUT} causes a current I_{PG} to flow, which can be calculated using the following equation:

$$I_{PG} = \left(\frac{V_{REF} - V_{OUT}}{R_{PG} + 1k\Omega}\right)$$

(Note: the 1kΩ term takes into account the effective output impedance of the voltage follower.)

I_{PG} is sensed internally and fed to a comparator with ±10µA threshold levels (with 1µA of hysteresis). The voltage tolerance V_{TOL} (= V_{REF} - V_{OUT}) can be set to the desired value by setting I_{PG} to 10µA in the above equation and solving for R_{PG}, as shown below:

$$R_{PG} = \left(\frac{V_{TOL}}{10\mu A}\right) - 1k\Omega$$

When the output voltage exceeds the tolerance limit, the STAT pin goes LOW. For example, to have a power good voltage threshold of 100mV, an R_{PG} value of 9kΩ would be used.

The capacitor C_{PG} connected to the PGIN pin serves to compensate the Power Good Amplifier. It is recommended that the minimum value of C_{PG} be 100pF. It is important to realize that the power good circuit monitors the difference between V_{REF} and V_{OUT}. In order to ensure proper power good functionality on startup, the soft start filter must adequately delay the output voltage from rising until the reference voltage has somewhat settled. For this reason, it is suggested that the $R_{REF} \bullet C_{REF}$ time constant be at least one order of magnitude smaller than the $R_{DES} \bullet C_{DES}$ time constant.

If the power good function is not needed, it can be disabled by connecting the PGIN pin to AVDD. In this case, R_{PG} and C_{PG} are not needed.

Voltage Margining

Voltage margining can be achieved by changing the current through R_{BIAS} where $I_{BIAS} = 1.23V/R_{BIAS}$. This current will be mirrored at R_{REF} to give an output voltage $V_{OUT} = I_{BIAS} \bullet R_{REF}$.

Changing the current I_{BIAS} can be done in two different ways; either by changing the values of RBIAS by using external switches or FETs driven by TTL signal (see Figure 5) or simply by applying a varying voltage through an additional resistor at IBIAS pin to form a current divider.

Regulator Status

The regulator status (STAT) signal provides an open-drain output, consistent with CMOS logic levels, that indicates whether the regulator is functioning properly. It should be externally pulled HIGH (using a pull-up resistor) during normal device operation, and is driven LOW when one or more of the following conditions exist:

- The regulator is not enabled, or has not yet completed its initial power-up sequencing.
- The power good circuit has detected that the output voltage is not within its programmed tolerance limits.
- The die temperature has exceeded a threshold of approximately 145°C.
- There is an open or short (to ground) on any one of the BIAS, IMAX, or IRIPL inputs. For the BIAS pin, the regulator immediately stops switching as well.
- UVLO for A_{VDD} has tripped.
- UVLO or OVLO for V_{DD} has tripped.
- V_{REF} becomes higher than A_{VDD} - 0.8V.
- V_{DD} becomes higher than A_{VDD} + 0.8V.
- The maximum average current setting has dropped below a preset level as described in the Maximum Output Current and Ripple Current Selection section.

Synchronous Rectification

This regulator utilizes the full benefits of a synchronous rectification topology. Both power FETs are integrated on chip, and no external Schottky diodes are required. During normal device operation, the low-side switch acts as a synchronous rectifier, carrying the output current that would normally flow through an external catch diode. This technique reduces losses associated with the diode's forward voltage drop. The subsequent power savings are especially advantageous in low-output-voltage applications.

Output Voltage Selection

The desired output voltage at the VDES pin can be applied externally or generated internally.

If the voltage is applied externally, proper operation of the power good circuit requires: 1) connection of the external reference to both the VREF and VDES pins, and 2) con-

a	b	V_{OUT}	R_{BIAS}
0	1	V_O	Rc//Rb
0	0	V_O - b%	Rc
1	1	V_O + a%	Rc//Ra//Rb
1	0	X	Rc//Ra

$$V_{OUT} = 1.23\left(\frac{R_{REF}}{R_{BIAS}}\right)$$

$$Ra = 43.2k\Omega\left(\frac{100}{a}\right)$$

$$Rb = 43.2k\Omega\left[\frac{1}{1 - \left(1 - \frac{b}{100}\right)}\right]$$

$$Rc = 43.2k\Omega\left[\frac{1}{\left(1 - \frac{b}{100}\right)}\right]$$

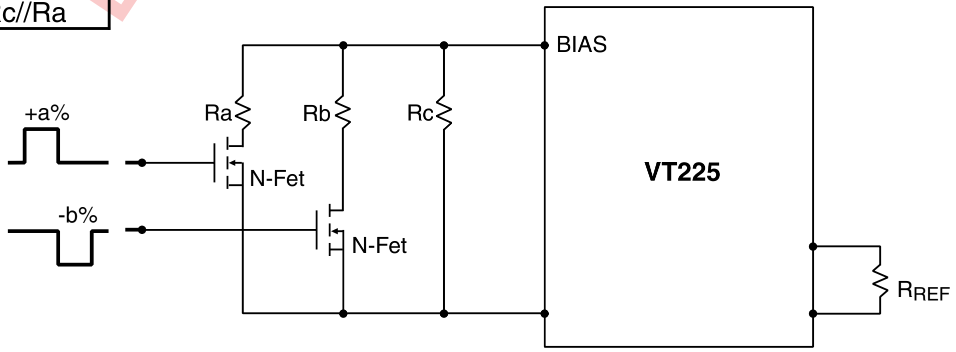


Figure 5. Voltage Margining Circuit with Logic Table

nection of the BIAS input to AVDD, disabling the internal current source driving the VREF pin.

To generate the desired voltage internally, simply select R_{REF} according to the equation:

$$V_{REF} = 1.23V \cdot \left(\frac{R_{REF}}{43.2k\Omega}\right)$$

The VREF pin is then connected to VDES through R_{DES} and C_{DES}.

Because of the reliance of external resistors to set bias currents and reference voltages, it is recommended to use the most accurate resistors available to ensure consistent regulation across operating conditions. For maximum accuracy, 0.1% accuracy resistors should be used.

In order to ensure proper operation of the internal VREF current mirror and error amplifier, the following restrictions should be observed:

- VDES should be set no lower than 0.5V.
- VDES should be set no higher than A_{VDD}-1.0V when generated internally.
- VDES should be set no higher than A_{VDD}-0.85V when generated externally.

If an output voltage higher than these limits is required (i.e., V_{OUT} = 2.5V with VDD = 3.3V±10%), then a voltage divider on V_{OUT} should be used to constrain the voltage on VFB so that VDES will be within the limits mentioned above.

For example, in the case with VDD = 3.3V and V_{OUT} = 2.5V, a feedback divider ratio of ½ can be used in order to keep VDES within the appropriate voltage restrictions relative to AVDD. Specifically, R_{REF} is chosen according to the equation, $V_{REF} = 1.23V \cdot (R_{REF}/43.2k\Omega)$, to program V_{REF} = 2.5V/2. In conjunction, the feedback divider comprised of R_{FB1} and R_{FB2} is set up for a ratio of ½ such that $R_{FB2}/(R_{FB1}+R_{FB2}) = ½$. In this case, $R_{FB1} = R_{FB2}$. Thus, R_{FB1} can be chosen for the desired droop amount according to:

$$V_{DROOP} = \left(\frac{R_{FB1}}{Ki}\right) \cdot I_{OUT}$$

and R_{FB2} is determined by the previous equation. Figure 6 illustrates the circuit configuration.

For setting "power good" thresholds, the PGIN pin should be utilized with the same divider ratio. In this case, for a ratio of ½, $R_{PG1} = R_{PG2}$. R_{PG1} depends on the voltage tolerance desired and is set by the following equation:

$$R_{PG1} = \left(\frac{V_{TOL}}{10\mu A}\right) - \left(\frac{1k\Omega}{\text{Divider Ratio}}\right)$$

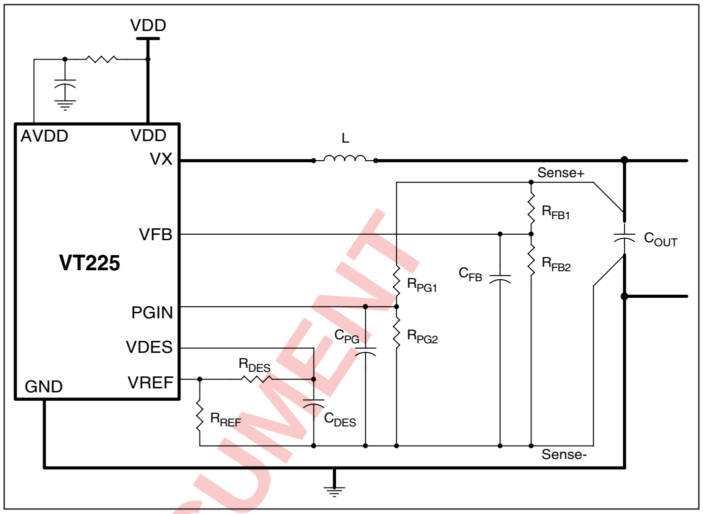


Figure 6. Configuration with Feedback Divider

Current Sharing

The droop generated across R_{FB} can be used to passively share current between two regulators within this family without any additional components. Larger values of droop will result in more accurate current sharing between regulators. A minimum full load droop of about 20mV is recommended. It is also easy to obtain preferential current sharing by choosing different values of R_{FB} for each regulator. For details in setting the droop voltage, refer to the Control Architecture section.

Zero Droop Operation

The high gain of the integrator in the error amplifier allows for operation with essentially zero static droop when $R_{FB} = 0\Omega$. Note that current sharing is not balanced with zero droop without the use of additional circuitry. Therefore, use nonzero values of R_{FB} for current sharing between multiple regulators. C_{FB} is not needed if $R_{FB} = 0\Omega$.

Local and Remote Output Voltage Sensing

To ensure the most accurate sensing of the output voltage, it is recommended that all components connected to the VREF, VDES, VFB and PGIN pins be configured as shown in Figure 2, so as to form SENSE+ and SENSE- lines. These SENSE lines support fully-differential voltage sensing and can be used in both local and remote sense applications. Point-of-load sensing helps compensate for voltage drops between the output of the regulator and its load, and provides the highest regulation accuracy.

EXTERNAL COMPONENT SELECTION

Table 1 provides a comprehensive list of external components required to complete the regulation system. More detailed information on component selection for the output filter is provided in the following sections.

Inductor Selection

The output inductor has an important influence on the overall size, cost, and efficiency of the voltage regulator. Smaller inductor values usually correspond to larger saturation current ratings, smaller physical sizes, or both. Since the inductor is typically one of the larger components in the system, a minimum inductor value is particularly important in space-constrained applications. Smaller inductor values also permit faster transient response.

For any buck regulator, the maximum current slew rate through the output inductor is given by:

$$\text{Slew Rate} = \frac{dI_L}{dt} = \frac{V_L}{L}$$

where I_L is the inductor current, L is the output inductance, and V_L is the voltage drop across the inductor. This equation implies that larger inductor values limit the regulator's ability to slew current through the output inductor in response to step load transients. Consequently, more output capacitors are required to supply (or store) sufficient charge to maintain regulation while the inductor current "catches up" to the load.

In contrast, smaller inductor values increase the regulator's maximum achievable slew rate and decrease the necessary capacitance, at the expense of higher ripple current. The peak-to-peak ripple current is given by the following equation:

$$I_{RIPL} = \left(\frac{V_{OUT}}{L \bullet f}\right) \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where f is the switching frequency, L is the output inductor value, V_{IN} is the input voltage, and V_{OUT} is the output voltage. From this equation, it is clear that for the same switching frequency, ripple current increases inversely as L decreases. This increased ripple current results in increased AC loss, larger peak current and, for the same output capacitance, results in increased output voltage ripple.

The saturation current rating of the inductor is another important consideration. In periodic steady-state at full load, the peak inductor current is given by:

$$I_{PK} = I_{MAX} + \frac{I_{RIPL}}{2}$$

where I_{MAX} is the maximum DC load current (see the Maximum Output Current and Ripple Current Selection section) and I_{RIPL} is the peak-to-peak inductor current ripple, defined above. For proper operation of the regulator, it is important that I_{PK} never exceeds the saturation current rating of the inductor, I_{SAT}, during steady-state operation. It is recommended that a margin of at least 20% is included between I_{PK} and I_{SAT}:

$$I_{SAT} > 1.2 \bullet I_{PK}$$

Table 1: Recommended External Components

Component	Value	Quantity	Comments
Input Capacitors	22µF or 10uF	1 or 2	X5R or X7R 6.3V
Input HF Bypass Capacitor	0.1µF	1	X5R 0603 size
AVDD Bypass Capacitor	0.1µF	1	X5R 0603 size
EN Bypass Capacitor	0.1µF	1	X5R 0603 size
C_{REF} Capacitor	100pF	1	X5R 0603 size
C_{DES} Capacitor	0.01µF	1	X5R 0603 size
C_{PG} Capacitor	0.01µF	1	X5R 0603 size
Output Capacitors Option 1	120µF	12 x 10µF Low Profile	X5R or X7R 6.3V
Output Capacitors Option 2	132µF	6 x 22µF Low Profile	X5R or X7R 6.3V
AVDD Resistor	10Ω	1	0603 size
R_{STAT} Resistor	10kΩ	1	0603 size
R_{MAX} Resistor	9.1kΩ	1	0603 size
R_{RIPL} Resistor	24kΩ	1	0603 size
R_{BIAS} Resistor	43.2kΩ 1%*	1	0603 size
R_{DES} Resistor	100kΩ	1	0603 size
R_{REF} Resistor	Set by App*	1	0603 size
R_{PG} Resistor	10kΩ	1	0603 size
Output Inductor	200nH	1	See Table 2

*0.1% thin-film resistors should be used for best DC accuracy.

For example, in a 5V to 1.5V application with f = 1MHz and L = 100nH, I_{RIPL} = 10.5A. With I_{MAX} programmed to 12A, the peak inductor current is I_{PK} = 17.3A, and an inductor with a saturation current rating of at least 21A is recommended. Also note that the saturation current of an inductor is generally smaller at high temperature than at room temperature. It is therefore recommended that the saturation current of the inductor be specified at the maximum case temperature of 125^{o}C.

Finally, the power dissipation of the inductor influences the regulation efficiency. Losses in the inductor include core loss, DC resistance loss, and AC resistance loss. For the best efficiency, inductors with ferrite core material exhibit-

Table 2: Inductor Suppliers

Company	Value (nH)	I_{SAT}	R_{DC} (mΩ)	Footprint (mm)	Height (mm)	Part Number	Phone	Website
Cooper Electronics	50	60A*	0.46	7.2 x 6.7	5	FP2-V050	(561) 752-5000	www.cooperet.com
	100	29A	0.47	7.2 x 6.7	5	FP2-V100		
	150	28A	0.59	10.2 x 6.8	5	FP4-150		
	200	20A	0.58	10.2 x 6.8	5	FP4-200		
ICE Components	50	60A*	0.37	7.2 x 6.5	5.2	LP02-500-1S	(800) 729-2099	www.icecomponents.com
	85	44A	0.35	7.2 x 6.5	5.2	LP02-800-1S		
	95	32A	0.46	7.0 x 6.5	5	LP02-101-1		
	155	31A	0.44	9.0 x 7.0	5	LP02-151-2		
	210	22A	0.41	9.0 x 7.0	5	LP02-201-2		
Pulse	72	48A	0.45	7.0 x 7.0	5	PA0512.700	(858) 674-8159	www.pulseeng.com
	105	34A	0.46	7.0 x 7.0	5	PA0512.101		
	150	21A	0.44	7.0 x 7.0	5	PA0512.151		
	155	32A	0.55	10.2 x 7.0	5	PA0511.151		
	220	23A	0.58	10.2 x 7.0	5	PA0511.221		
Toko	50	49A	0.72	7.4 x 6.7	5	FDN0650-500	(408) 432-8281	www.tokoam.com
Vishay-Dale	100	39A	2.90	7.0 x 6.5	3	IHLP-2525CZ-01 0.1	(605) 665-9301	www.vishay.com
	200	33A	3.35	7.0 x 6.5	3	IHLP-2525CZ-01 0.2		
	470	19A	5.62	7.0 x 6.5	3	IHLP-2525CZ-01 0.47		
Vitec	50	52A	0.29	7.6 x 7.5	5	59P9002	(760) 918-8831	www.viteccorp.com
	70	45A	0.30	7.6 x 7.5	5	59P9003		
	100	28A	0.33	7.6 x 7.5	5	59P9022		
	100	23A	0.75	9.2 x 9.2	2.3	59P9071		
	100	31A	0.48	9.2 x 9.2	3.7	59P9073		
	200	22A	1.29	7.7 x 7.4	4.2	59P9051		
	200	16A	2.08	5.0 x 5.0	5	59P9090		
	470	11A	2.43	7.7 x 7.4	4	59P9052		
	470	11A	4.92	5.0 x 5.0	5	59P9091		

***** Inductance drop less than 20% for I_{DC} up to 60A.

NOTE 2: Saturation current (I_{SAT}) and DC winding resistance (R_{DC}) as characterized by Volterra at 125°C.

NOTE 3: I_{SAT} is defined by Volterra as a 20% drop in zero-bias inductance at 125°C.

NOTE 4: 50nH inductors result in large ripple currents and are recommended for use at low-voltage and/or high switching frequency.

ing low loss in the range of 0.5MHz to 2MHz, DC winding resistance below 1.5mΩ, and AC winding resistance below 15mΩ at 2MHz are recommended.

Table 2 provides a summary of recommended inductor suppliers and part numbers. Each inductor meets the electrical requirements of the VT225 applications and has been characterized and guard-banded by Volterra to specify minimum saturation current at 125°C over part-to-part and lot-to-lot variations. In addition, most of these inductors share a common printed circuit board (PCB) footprint, simplifying parts procurement.

The choice of 100nH-200nH inductors with switching frequencies in the range of 700kHz to 1.5MHz are generally recommended as a good trade-off between efficiency, transient response, current ripple, voltage ripple and overall system size in a typical 5V to low-voltage application with the VT225. For applications with the most demanding transient requirements, 50nH inductors and switching frequencies above 1MHz are recommended. For output voltages above 2V and/or for higher efficiency, physically larger 200nH inductors are recommended.

Ouput Capacitor Selection

Output capacitance is selected to provide suitable transient tolerance and output voltage ripple. For the best performance, lowest cost, and smallest size of the VT225 systems, multilayer ceramic chip (MLCC) capacitors with 1210 or smaller case sizes, capacitance values of 47µF or smaller, 6.3V voltage ratings, and X5R or better temperature characteristics are recommended.

In VT225 systems with large transient load steps and MLCC output capacitors, it is generally the value of capacitance, rather than the series parasitics of those capacitors, that determines the transient tolerance. The minimum recommended value of 132µF has been chosen so that over the entire input and output voltage range, the output voltage will not deviate by more than 50mV from its nominal value during a 6A load current step, assuming an output current slew rate no greater than 300A/µs, and a 200nH inductor. The minimum recommended value of capacitance scales inversely with maximum output current. The VT225, for example, requires only 132µF of output capacitance.

If desired, more capacitance can be added at the output to tighten transient tolerance at the expense of increased size, cost, and component count. For a given load step magnitude ΔI_{LOAD}, output inductor value L, peak-to-peak ripple current I_{RIPL}, input voltage V_{IN} and output voltage V_{OUT}, the transient overshoot and undershoot generally scale inversely with the value of output capacitance, C_{OUT}. For larger load steps with the same tolerance, capacitance should be increased with load step magnitude and peak-to-peak ripple current according to the following relationship:

$$C_{OUT} \propto \left(\Delta I_{LOAD} + \frac{I_{RIPL}}{2}\right)^2$$

The voltage undershoot associated with a loading transient generally scales inversely with (V_{IN} - V_{OUT}). Similarly, the voltage overshoot associated with an unloading transient scales inversely with V_{OUT}. For the same transient tolerance, C_{OUT} generally scales linearly with L (see the Inductor Selection section).

The transient tolerance of a VT225 system is ultimately limited by the finite high-frequency transconductance of the integrated error amplifier. The Error Amplifier Operation section of this datasheet provides a description of the phenomenon and a closed-form expression to predict the minimum achievable transient undershoot and overshoot. With a 12A load step and nominal Ki of 120,000, the transient tolerance is limited to approximately 33mV. This transient tolerance improves linearly with decreasing load step magnitude and increasing Ki.

Output voltage ripple is another important consideration in the selection of output capacitors. For a buck regulator operating in continuous conduction mode, the total voltage ripple across the output capacitor bank can be approximated as the sum of three voltage waveforms: 1) the triangle wave that results from multiplying the AC ripple current by the ESR, 2) the square wave that results from multiplying the ripple current slew rate by the ESL, and 3) the piecewise quadratic waveform that results from charging and discharging the output capacitor. Although the phasing of these three components does impact the total output ripple, a common approximation is to ignore the phasing and to find the upper bound of the peak-to-peak ripple by summing all three components:

$$V_{PP} = (ESR)(I_{RPIL}) + (ESL)\left(\frac{V_{IN}}{L}\right) + \left(\frac{I_{RIPL}}{8fC_{OUT}}\right)$$

where ESR is the equivalent series resistance at the output, I_{RIPL} is the peak-to-peak inductor current ripple, ESL is the high-frequency equivalent series inductance at the output, V_{IN} is the input voltage, L is the output inductance, f is the switching frequency, and C_{OUT} is the output capacitance. In a typical VT225 application with a bank of 1210 X5R 6.3V 22µF output capacitors, these three components are roughly equal.

The ESL effect of an output capacitor on output voltage ripple cannot be estimated from the resonant frequency, but from the high-frequency (10MHz or above) impedance of that capacitor. The contribution to ESL of a single 1210 22µF output capacitor is between 0.2 and 0.3nH, rather than the 1.2nH usually quoted. PCB traces and vias in the V_{OUT} / GND loop contribute additional parasitic inductance.

Although MLCCs offer the highest performance of any capacitor technology, they can exhibit resonance effects at multiple frequencies that fall within the switching frequency range of the regulator. Under some conditions, this resonance can affect the switching behavior, causing a nonlinear relationship between R_{RIPL} and switching frequency. To help reduce the impact of MLCC resonance on overall regulator performance, Volterra recommends using low profile 22µF MLCCs (see Table 3 for those capacitors with nominal thickness less than 2mm). Increasing the amount of output capacitance will also help reduce the effects of MLCC resonance.

The final considerations in the selection of output capacitors are ripple current rating and power dissipation. Using a conservative design approach, the output capacitors should be designed to handle the maximum peak-to-peak AC ripple current experienced in the worst case. Because the recommended output capacitors have extremely low ESR values, they easily satisfy this ripple current requirement. For the triangular AC ripple current at the output, the total RMS current that needs to be handled is calculated as:

$$I_{RMS_{COUT}} = \frac{I_{RIPL}}{\sqrt{12}}$$

and the total power dissipation in the output capacitors is:

$$P_{COUT} = I^2_{RMS_{COUT}} \cdot ESR$$

where ESR is the equivalent series resistance of the entire output capacitor bank. In a 5V to 1.5V application using a 200nH output inductor and switching at 1MHz, the peak-to-peak ripple current is 5.3A, yielding an RMS ripple current of 1.5A. With six 22µF output capacitors in the 1210 case size (C_{OUT} = 132µF and ESR = 1mΩ total), each capacitor must handle a worst-case RMS ripple current of (1.5/6 = 0.25A). Using the recommended output capacitors, this RMS current level corresponds to a total power dissipation of 2mW and surface temperature rise of less than 1°C, and thus falls well within the ripple current rating for the parts. Operation

Table 3: Output Capacitor Suppliers

Company	Value (µF)	Part Number	Temp. Rating	Volt. Rating	Case Size	t [5]	Phone	Website
AVX	47	12064D476MAT2A	X5R	4V	1206	1.65	(843) 448-9411	www.avxcorp.com
	47	12106D476MAT2A	X5R	6.3V	1210	2.45		
	22	08054D226MAT2A	X5R	4V	0805	1.3		
	22	12066D226MAT2A	X5R	6.3V	1206	1.65		
	10	08056D106MAT2A	X5R	6.3V	0805	1.3		
	10	1206D106MAT2A	X5R	6.3V	1206	1.65		
Murata	47	GRM31CR60J476ME19L	X5R	6.3V	1206	1.6	(770) 436-1300	www.murata.co.jp
	47	GRM32ER60J476ME20L	X5R	6.3V	1210	2.5		
	22	GRM21BR60J226ME39L	X5R	6.3V	0805	1.25		
	22	GRM31CR60J226KE19L	X5R	6.3V	1206	1.6		
	22	GRM32DR60J226KA01L	X5R	6.3V	1210	2.0		
	10	GRM219R60J106KE19D	X5R	6.3V	0805	0.85 [6]		
	10	GRM31MR60J106KE01L	X5R	6.3V	1206	1.6		
Panasonic	47	ECJ3YB0J476M	X5R	6.3V	1206	1.6	(714) 373-7334	www.panasonic.com
	47	ECJ4YB0J476M	X5R	6.3V	1210	2.4		
	22	ECJ3YB0J226M	X5R	6.3V	1206	1.6		
	22	ECJHVB0J226M	X5R	6.3V	1206	0.85 [6]		
	10	ECJ2FB0J106M	X5R	6.3V	0805	1.25		
	10	ECJ3YB0J106M	X5R	6.3V	1206	1.6		
Taiyo Yuden	47	AMK316BJ476ML	X5R	4V	1206	1.6	(408) 753-4150	www.taiyo-yuden.com
	47	JMK325BJ476MM	X5R	6.3V	1210	2.5		
	22	AMK212BJ226MG	X5R	4V	0805	1.25		
	22	JMK316BJ226ML	X5R	6.3V	1206	1.6		
	22	JMK325BJ226MY	X5R	6.3V	1210	1.9		
	10	JMK212BJ106MD	X5R	6.3V	0805	0.85 [6]		
	10	JMK316BJ106ML	X5R	6.3V	1206	1.6		
TDK	47	C3216X5R0J476M	X5R	6.3V	1206	1.6	(847) 803-6100	www.component.tdk.com
	47	C3225X5R0J476M	X5R	6.3V	1210	2.5		
	22	C2012X5R0J226M	X5R	6.3V	0805	1.25		
	22	C3216X5R0J226M	X5R	6.3V	1206	1.6		
	22	C3225X5R0J226M	X5R	6.3V	1210	1.6		
	10	C2012X5R0J106M	X5R	6.3V	0805	1.25		
	10	C3216X5R0J106M	X5R	6.3V	1206	1.6		

NOTE 5: t indicates nominal thickness in mm.
NOTE 6: Indicates capacitors with nominal thickness smaller than the minimum CSP package thickness.

under such conservative conditions extends the lifetime of the capacitors and improves system reliability.

Table 3 provides a list of recommended output capacitors for VT225 systems. Each capacitor has 1210 or smaller case size, X5R or better temperature rating, 6.3V or 4V voltage rating and value of 47µF or smaller.

Input Capacitor Selection

The selection and placement of input capacitors are important considerations. High-frequency input capacitors serve to control switching noise. Bulk input capacitors are designed to absorb the pulsed DC current that is drawn by the regulator. For the best performance, lowest cost, and smallest size of the VT225 system, multi-layer ceramic chip (MLCC) capacitors with 1210 or smaller case sizes, capacitance values of 22µF or smaller, 6.3V or 10V voltage ratings and X5R or better temperature characteristics are recommended as bulk. The minimum recommended value of capacitance is 20µF (bulk) and 0.1µF (high-frequency).

Because the bulk input capacitors must source the pulsed DC input current of the regulator, the power dissipation and ripple current rating for these capacitors are far more important than that for the output capacitors. The magnitude of the RMS input capacitor current can be approximated using the following equation:

$$I_{RMS_{CIN}} = \frac{I_{LOAD}\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

Table 4: 6.3V Input Capacitors Suppliers

Company	Value (µF)	Part Number	Temp. Rating	Volt. Rating	Case Size	t [7]	Phone	Website
AVX	22	12066D226MAT2A	X5R	6.3V	1206	1.65	(843) 448-9411	www.avxcorp.com
	10	08056D106MAT2A	X5R	6.3V	0805	1.3		
	4.7	06036D475KAT2A	X5R	6.3V	0603	0.85 [8]		
Murata	22	GRM21BR60J226ME39L	X5R	6.3V	0805	1.25	(770) 436-1300	www.murata.co.jp
	22	GRM31CR60J226KE19L	X5R	6.3V	1206	1.6		
	10	GRM219R60J106KE19D	X5R	6.3V	0805	0.85 [8]		
	4.7	GRM188R60J475KE19D	X5R	6.3V	0603	0.8 [8]		
Panasonic	22	ECJHVB0J226M	X5R	6.3V	1206	0.85 [8]	(714) 373-7334	www.panasonic.com
	22	ECJ3Y70J226M	X7S	6.3V	1206	1.6		
	10	ECJGVB0J106M	X5R	6.3V	0805	0.85 [8]		
	10	ECJ2F70J106M	X7S	6.3V	0805	1.25		
	4.7	ECJ1VB0J475M	X5R	6.3V	0603	0.8 [8]		
Taiyo Yuden	22	JMK316BJ226ML	X5R	6.3V	1206	1.6	(408) 753-4150	www.taiyo-yuden.com
	10	JMK212BJ106MD	X5R	6.3V	0805	0.85 [8]		
	10	JMK316BJ106MD	X5R	6.3V	1206	0.85 [8]		
	10	JMK316BJ106ML	X7R	6.3V	1206	1.6		
	4.7	JMK107BJ475MA	X5R	6.3V	0603	0.8 [8]		
TDK	22	C2012X5R0J226M	X5R	6.3V	0805	1.25	(847) 803-6100	www.component.tdk.com
	22	C3216X6S0J226M	X6S	6.3V	1206	1.6		
	10	C2012X5R0J106M	X5R	6.3V	0805	1.25		

NOTE 7: t indicates nominal thickness in mm.
NOTE 8: Indicates capacitors with nominal thickness smaller than the minimum CSP package thickness.

where I_{LOAD} is the output DC load current. With an equivalent series resistance of the bulk input capacitor bank, ESR_{CIN}, the total power dissipation in the input capacitors is:

$$P_{CIN} = I^2_{RMS_{CIN}} \cdot ESR_{CIN}$$

For a VT225 system converting 5V to 1.5V with 12A of load current, the RMS current flowing through the input capacitor bank is equal to 5.5A. If two 10µF input capacitors in 1206 cases are used, the overall bulk capacitance is 20µF and the overall ESR is 4mΩ. The power dissipation in the input capacitors is 120mW, yielding nearly 10°C in case temperature rise. For better performance and increased reliability, the number of bulk input capacitors should be increased to three or more.

The proximity of the input capacitors to the VT225 can have an important impact on efficiency and regulation. For optimum performance, the VDD rows should have 0.1µF high-frequency bypass and bulk input capacitance tied to the ground plane as close to the chip as possible. An uninterrupted ground plane should be used directly beneath the VDD traces which run from the input capacitors to the chip to minimize parasitic inductance.

Table 4 provides a list of recommended bulk input capacitors for VT225 systems. Each capacitor has 1210 or smaller case size, X5R or better temperature rating and 6.3V voltage rating.

Resistor Selection and its Effect on DC Output Voltage Accuracy

The desired output voltage, V_{REF}, is set using resistors R_{BIAS} = 43.2kΩ and R_{REF} according to the following equation:

$$V_{REF} = V_{BG} \cdot \left(\frac{R_{REF}}{R_{BIAS}}\right)$$

where V_{BG} = 1.23V ±1% over input voltage and temperature, and R_{REF} and R_{BIAS} have manufacturer specified resistance tolerances and temperature coefficients. The error amplifier of the VT225 compares the output voltage to V_{REF} to create an appropriate error signal for regulation. This error amplifier includes input-referred DC offset with zero mean and absolute tolerance guaranteed to ±3.5mV over input voltage and temperature. Figure 7 plots the DC accuracy of the regulator's output voltage ($V_{OUT} = V_{REF}$ ±DC Accuracy) assuming ideal R_{REF} and R_{BIAS}.

Nonidealities in R_{REF} and R_{BIAS} contribute additional error. Table 5 and Table 6 show the absolute worst-case contribution of resistor tolerance and temperature coefficient (over a 100°C temperature range) to output voltage accuracy. These numbers are added directly to those of Figure 7 to obtain the overall output voltage accuracy. For example, with 0.1% resistor tolerance and ±25ppm/°C temperature coefficient, the DC accuracy at a 1.5V output voltage is ±1.2% from the chip, ±0.2% from the resistor tolerance and ±0.5% from the resistor temperature coefficient, yielding ±1.9% overall. If the same design were to use lower cost resistors with 1% tolerance and ±100ppm/°C temperature coefficient, the DC accuracy would be reduced to 5.2%.

Volterra has partnered with two thin-film resistor manufacturers to create cost-effective 0.1% tolerance, ±25ppm/°C resistors in 0603 case sizes. The two values enabled are 41.2kΩ and 115kΩ, although other values are available upon request from these manufacturers. The part numbers and contact information for these two sources are listed in Table 7.

Printed Circuit Board Layout

The printed circuit board layout can dramatically affect the performance of the regulator. A poorly designed board can degrade efficiency, noise performance, and even control loop stability. At higher switching frequencies, layout issues are especially critical.

As a general guideline, the input capacitors and the output inductor should be placed in close proximity to the regulator IC, while the output capacitors should be lumped together as close to the load as possible. Traces to these components should be kept as short and wide as possible to minimize parasitic inductance and resistance. Traces connecting the input capacitors and internal FETs on the IC require particular attention since they carry currents with the largest RMS values and fastest slew rates. The input capacitors should be placed as close to the input supply pins as possible. Preferably, there should be an uninterrupted ground plane located immediately underneath these high-frequency current paths, with the ground plane located no more than 8 mils below the top layer. By keeping the flow of this high-frequency AC current localized to a tight loop at the regulator, electromagnetic interference (EMI) can be minimized.

Voltage sense lines should be routed differentially directly from the load points. They should be routed in parallel and in close proximity to each other with common-mode filtering to the AGND pin of the IC or a quiet section of the ground plane. The ground plane can be used as a shield for these or other sensitive signals to protect them from capacitive or magnetic coupling of high-frequency noise.

For remote-sense applications where the load and regulator IC are separated by a significant distance or impedance, it is important to place the majority of the output capacitors directly at the load. Ideally, for system stability, all of the output capacitors should be placed as close as possible to the load. In remote-sense applications, common-mode filtering is necessary to filter high-frequency noise in the sense lines.

Table 5: DC Output Voltage Accuracy versus R_{REF} and R_{BIAS} Tolerance

Resistor Tolerance	DC Output Voltage Accuracy
±0.1%	±0.2%
±0.5%	±1.0%
±1.0%	±2.0%

Table 6: DC Output Voltage Accuracy versus R_{REF} and R_{BIAS} Temperature Coefficient

Resistor Temperature Coefficient	DC Output Voltage Accuracy
±25ppm/°C	±0.5%
±50ppm/°C	±1.0%
±100ppm/°C	±2.0%

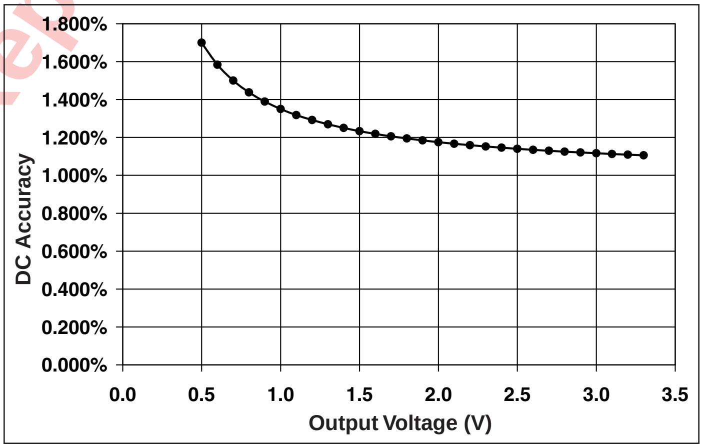


Figure 7. DC Accuracy of VT225 IC with Ideal R_{REF} & R_{BIAS}

Table 7: Thin-Film Resistor Suppliers

Company	Value	Accuracy	Temp. Coefficient	Case Size	Part Number	Phone	Website
Thin Film Technology	41.2kΩ 115kΩ	±0.1% ±0.1%	±25ppm/°C ±25ppm/°C	0603 0603	RR0816P4122B-T5 RR0816P1153B-T5	(507) 625-8445	www.thin-film.com
Venkel Ltd.	41.2kΩ 115kΩ	±0.1% ±0.1%	±25ppm/°C ±25ppm/°C	0603 0603	TFC0603-16W-E-4122BT TFC0603-16W-E-1153BT	(800) 950-8365	www.venkel.com

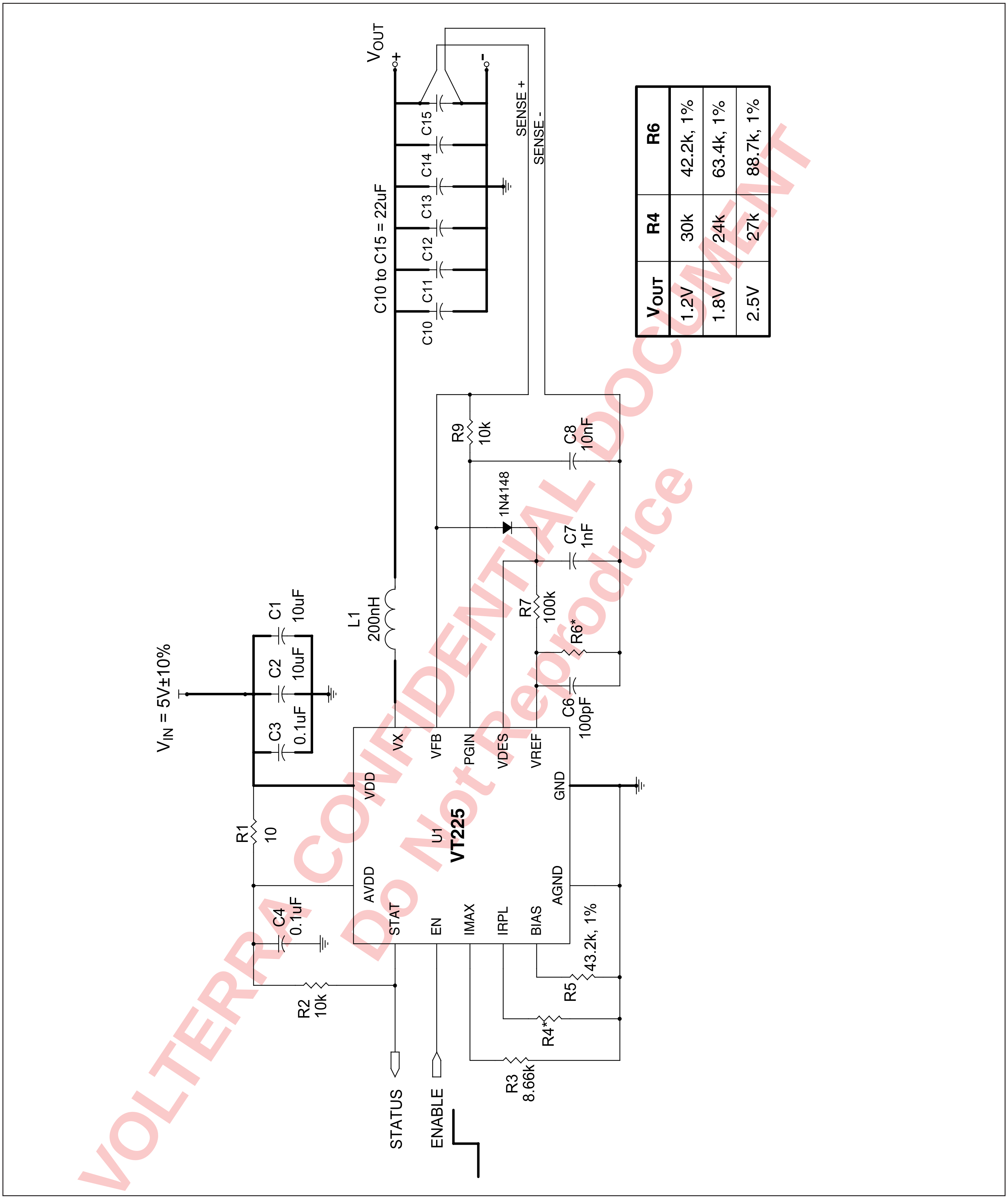
The following layout recommendations should be used for optimal performance:

- A low impedance ground plane is essential to keep all voltages referenced to a common ground.
- Multiple vias are recommended for all paths that carry high currents (i.e., ground, VDD, VX). Vias should be placed close to the chip to create the shortest possible current loops. Make sure via placement does not obstruct the flow of currents or mirror currents in the ground plane.
- Because the VT225 utilizes its AGND balls for accurate reference and bias purposes, the GND and AGND sections should be separated on the top layer of the PCB. AGND should then be tied through a via to a quiet area of the ground plane in close proximity to the chip. Typically, the area directly next to the AGND ball is the most convenient spot (i.e., next to H7 in the pinout diagram of the VT225).
- The capacitor that bypasses AVDD should have its ground terminal tied directly to the ground plane with a single via, creating the shortest possible current loop between it and the chip.
- Alternatively, AGND can be shorted directly to GND on the top layer (i.e., for the VT225, directly shorting balls H5-H7 to balls G4-G7). In this case, the ground terminal of the AVDD bypass capacitor should not be connected to the ground plane, but should be routed separately to the AGND ball.
- It is recommended that AGND be treated as a separate signal and routed in as short a distance as possible to the resistors tied to the BIAS, IMAX, and IRIPL outputs and to the common-mode filter capacitance on the sense lines. It is important that these AGND lines do not connect to GND at any place other than at the AGND ball.

Gerber files with layout information and complete reference designs can be obtained by contacting a Volterra account representative.

INTEGRATED, STEP-DOWN SWITCHING REGULATOR

TYPICAL APPLICATIONS



V_{OUT}	R4	R6
1.2V	30k	42.2k, 1%
1.8V	24k	63.4k, 1%
2.5V	27k	88.7k, 1%

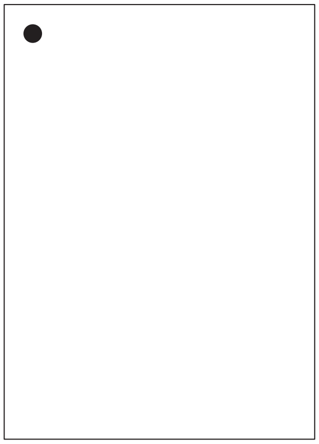
Figure 8. Reference Schematic (no droop)

INTEGRATED, STEP-DOWN SWITCHING REGULATOR

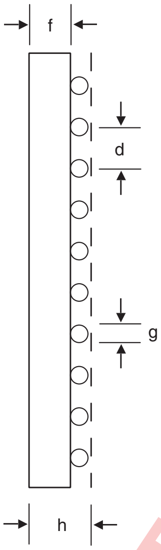
PACKAGE DIMENSIONS

VOLTERRA	Title: Package Outline - 62 Ball CSP VT225	Doc No. ES AP-0652	Rev. 0
		Page 1 of 2	

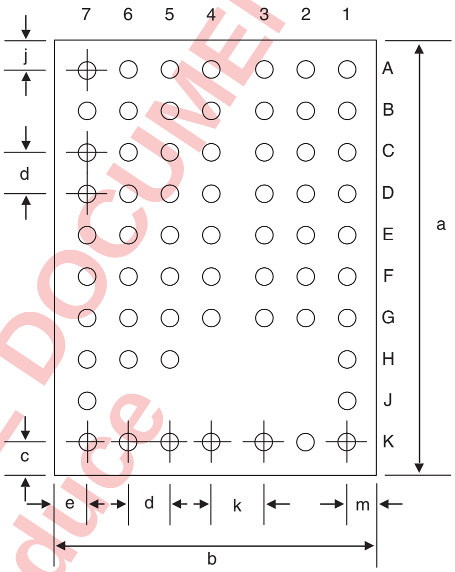
TOP VIEW



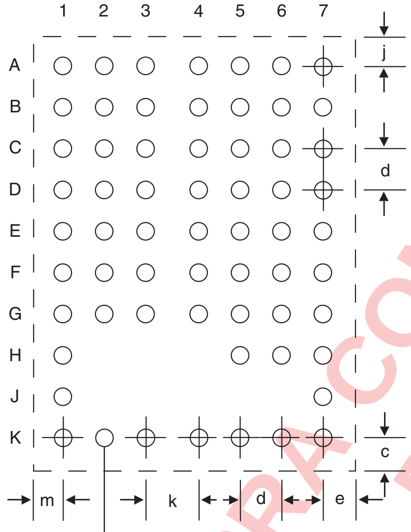
SIDE VIEW



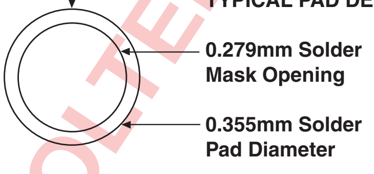
BOTTOM VIEW



LAND PATTERN



TYPICAL PAD DESIGN



	MILLIMETERS			INCHES[†]		
DIM	MIN	TYP	MAX	MIN	TYP	MAX
a	5.0850		5.1350	0.2002		0.2022
b	3.7410		3.7910	0.1473		0.1493
c		0.3067			0.0121	
d[‡]		0.5000			0.0197	
e		0.3359			0.0132	
f	0.6350		0.6850	0.0250		0.0270
g		0.3750			0.0148	
h		0.9500			0.0374	
j		0.3033			0.0119	
k[‡]		0.6000			0.0236	
m		0.3301			0.0130	

[†] *Inches provided for reference only.*

[‡] ***IMPORTANT: Ball pitch between columns 3 & 4 is 0.6000mm. All other columns and rows have 0.5000mm ball pitch.***

Notes

1. Drawings not to scale.
2. Ball pitch between columns 3 & 4 is 0.600mm. All other columns and rows have 0.500mm ball pitch.
3. Controlling dimensions are in millimeters.

DATASHEET PHASE DEFINITIONS

PRODUCT PREVIEW: Specifications are to be used as design targets for planning purposes as product is still in development stage.

PRELIMINARY: Specifications are based on limited product and system characterization as product is sampling and has not competed qualification.

NEW PRODUCT: Specifications are based on product and system characterization over all operating conditions as product has passed qualification and released to production.

FINAL: Specifications are based on volume manufacturing data and extensive field data as product has been in production over a year.

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NOTE

Always check with Volterra Semiconductor Corporation for the latest datasheet before completing a design.

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